

WHAT IS CLAIMED IS:

1. A magnetic random access memory device comprising:

5 a memory cell array in which a plurality of memory cells two-dimensionally arranged in a row direction and a column direction and each composed of a magneto-resistive effect element;

10 a plurality of first write lines each of which is provided along a row direction of the memory cell array and generates a magnetic field in a row direction of the memory cell array when a pulse-like first write current is applied to the plurality of first write lines along the row direction;

15 a plurality of second write lines each of which is provided along a column direction of the memory cell array and generates a magnetic field in a column direction of the memory cell array when a pulse-like second write current is applied to the plurality of second write lines along the column direction of the memory cell array, data being written in each memory cell by applying a combined magnetic field of the magnetic field generated in the column direction and the magnetic field generated in the row direction; and

25 a control circuit connected to the plurality of first and second write lines to control a dependence on temperature of a pulse width of at least one of the first write current and second write current.

2. A magnetic random access memory device according to claim 1, wherein the control circuit controls the temperature dependence of the pulse width so that the pulse width of the at least one of the 5 write currents is independent of temperature.

3. A magnetic random access memory device according to claim 1, wherein the control circuit controls the temperature dependence of the pulse width so that the pulse width of the at least one of the 10 write currents increases consistently with temperature.

4. A magnetic random access memory device according to claim 3, wherein the control circuit provides control such that a time for which the second write current is applied varies depending on data 15 written in the memory cell.

5. A magnetic random access memory device according to claim 3, wherein the control circuit provides control such that a time for which the first write current is applied differs from the time for 20 which the second write current is applied, in accordance with the data written in the memory cell.

6. A magnetic random access memory device according to claim 3, wherein the control circuit controls the magnitude of the at least one of the first 25 and second write currents to vary between a front edge and/or rear edge and a central portion of the pulse width.

7. A magnetic random access memory device according to claim 3, wherein the control circuit controls the time for which the at least one of the write currents is applied to decrease with increasing 5 temperature.

8. A magnetic random access memory device according to claim 3, wherein the control circuit controls a temperature dependence of the time for which the first write current is applied to differ from a 10 temperature dependence of the time for which the second write current is applied.

9. A magnetic random access memory device according to claim 2, wherein the control circuit controls a timing for starting application of the first 15 write current and a timing for starting application of the second write current as well as a timing for ending the application of the first write current and a timing for ending the application of the second write current to vary with temperature.

20 10. A magnetic random access memory device according to claim 3, wherein the control circuit adjusts a relationship between the timing for starting the application of the first write current and the timing for starting the application of the second write 25 current and a relationship between the timing for ending the application of the first write current and the timing for ending the application of the second

write current.

11. A magnetic random access memory device according to claim 10, further comprising a storage element that stores, in a nonvolatile manner, 5 information used to control the timings for applying the first and second currents.

12. A magnetic random access memory device according to claim 11, wherein the storage element is a laser blow fuse element.

10 13. A magnetic random access memory device according to claim 11, wherein the storage element is a tunnel magnetoresistive element.

15 14. A magnetic random access memory device according to claim 11, wherein the storage element is an anti-fuse that stores data depending on whether or not the tunnel magnetoresistive element is dielectrically broken down.

15. A magnetic random access memory device according to claim 2, further comprising:

20 a first driver connected to the plurality of first write lines to supply the first write current;

a second driver connected to the plurality of second write lines to supply the second write current;

25 a first sinker connected to the plurality of first write lines to sink the first write current;

a second sinker connected to the plurality of second write lines to sink the second write current;

a setting circuit which is connected to the control circuit and in which first setting data used to control a current waveform of the first write current and second setting data used to control a current waveform of the second write current are registered;

5 a first trigger circuit connected to the first driver and the first sinker to generate a first trigger signal to control the first driver and the first sinker; and

10 a second trigger circuit connected to the second driver and the second sinker to generate a second trigger signal to control the second driver and the second sinker,

15 wherein the control circuit receives the first and second setting data or data obtained by decoding the first and second setting data, and controls at least one of the first trigger circuit and second trigger circuit on the basis of these data to control at least one of the time for which the write currents are applied by the first driver and the second driver, respectively, the application timings, the magnitude of the write current, and the waveform of the write current.

20 16. A magnetic random access memory device according to claim 15, wherein the first sinker finishes operations a specified period after the first driver has finished operations.

17. A magnetic random access memory device according to claim 15, wherein the second sinker finishes operations a specified period after the second driver has finished operations.

5 18. A magnetic random access memory device according to claim 15, wherein the first trigger circuit has a first delay circuit for which a delay time is set in accordance with a value of an input current, and the first trigger circuit receives a write signal to generate, on the basis of the write signal, the first trigger signal having a period corresponding to the delay time of the first delay circuit, and
10 the second trigger circuit has a second delay circuit for which a delay time is set in accordance with the value of the input current, and the second trigger circuit receives the write signal to generate, on the basis of the write signal, the second trigger signal having a period corresponding to the delay time of the second delay circuit.

15 20. A magnetic random access memory device according to claim 18, further comprising a current source circuit which outputs and supplies the input current to the first and second trigger circuits.

20 25. A magnetic random access memory device according to claim 19, wherein the input current generated by the current source circuit is independent of temperature.

21. A magnetic random access memory device according to claim 19, wherein the current source circuit includes:

5 a first current source which outputs a first current having a value increasing in proportion to temperature;

a second current source which outputs a second current having a value decreasing in proportion to temperature; and

10 a current summing circuit which adds up the first and second currents to generate the input current.

22. A magnetic random access memory device according to claim 3, further comprising:

15 a first driver connected to the plurality of first write lines to supply the first write current;

a second driver connected to the plurality of second write lines to supply the second write current;

a first sinker connected to the plurality of first write lines to sink the first write current;

20 a second sinker connected to the plurality of second write lines to sink the second write current;

25 a setting circuit which is connected to the control circuit and in which first setting data used to control a current waveform of the first write current and second setting data used to control a current waveform of the second write current are registered;

a first trigger circuit connected to the first

driver and the first sinker to generate a first trigger signal to control the first driver and the first sinker; and

5 a second trigger circuit connected to the second driver and the second sinker to generate a second trigger signal to control the second driver and the second sinker,

10 wherein the control circuit receives the first and second setting data or data obtained by decoding the first and second setting data, and controls at least one of the first trigger circuit and second trigger circuit on the basis of these data to control at least one of the time for which the write currents are applied by the first driver and the second driver, 15 respectively, the application timings, the magnitude of the write current, and the waveform of the write current.

23. A magnetic random access memory device according to claim 22, wherein the first sinker 20 finishes operations a specified period after the first driver has finished operations.

24. A magnetic random access memory device according to claim 22, wherein the second sinker 25 finishes operations a specified period after the second driver has finished operations.

25. A magnetic random access memory device according to claim 22, wherein the first trigger

circuit has a first delay circuit for which a delay time is set in accordance with a value of an input current, and the first trigger circuit receives a write signal to generate, on the basis of the write signal, 5 the first trigger signal having a period corresponding to the delay time of the first delay circuit, and

the second trigger circuit has a second delay circuit for which a delay time is set in accordance with the value of the input current, and the second 10 trigger circuit receives the write signal to generate, on the basis of the write signal, the second trigger signal having a period corresponding to the delay time of the second delay circuit.

26. A magnetic random access memory device 15 according to claim 25, further comprising a current source circuit which generates and supplies the input current to the first and second trigger circuits.

27. A magnetic random access memory device according to claim 26, wherein the input current 20 generated by the current source circuit has a temperature dependence that the value of the input current increases consistently with temperature.

28. A magnetic random access memory device according to claim 27, wherein the current source 25 circuit includes:

a first current source which outputs a first current having a value increasing in proportion to

temperature;

a second current source which outputs a second current having a value decreasing in proportion to temperature; and

5 a current subtraction circuit which subtracts the second current from the first current to generate the input current.

29. A magnetic random access memory device according to claim 26, wherein the temperature 10 dependence of the input current from the current source circuit is exhibited as a folded line.

30. A magnetic random access memory device according to claim 1, wherein the magnetoresistive element is a tunnel magnetoresistive element having a 15 tunnel barrier film sandwiched between two ferromagnetic layers.

31. A magnetic random access memory device according to claim 1, wherein the plurality of first 20 write lines are write word lines, and the plurality of second write lines are write bit lines.